| Pin Names | Description |
| :--- | :--- |
| CLKIN, $\overline{\text { CLKIN }}$ | Differential Clock Inputs |
| CLK $_{1-4}, \overline{\text { CLK }}_{1-4}$ | Differential Clock Outputs |
| TCLK | Test Clock Input $\dagger$ |
| CLKSEL | Clock Input Select $\dagger$ |

$\dagger$ TCLK and CLKSEL are single-ended inputs, with internal $50 \mathrm{k} \Omega$ pulldown resistors.

## Truth Table

| CLKSEL | CLKIN | CLKIN | TCLK | CLK $_{\mathbf{N}}$ | CLK $_{\mathbf{N}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L | L | H | X | L | H |
| L | H | L | X | H | L |
| H | X | X | L | L | H |
| H | X | X | H | H | L |

[^0]
## Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
Storage Temperature
Maximum Junction Temperature ( $T_{J}$ )
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
$+150^{\circ} \mathrm{C}$
$+175^{\circ} \mathrm{C}$
Case Temperature under Bias ( $\mathrm{T}_{\mathrm{C}}$ )
$\mathrm{V}_{\text {EE }}$ Pin Potential to Ground Pin Input Voltage (DC)
Output Current (DC Output HIGH)
$0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
-7.0 V to +0.5 V
$\mathrm{V}_{\mathrm{CC}}$ to +0.5 V
$-50 \mathrm{~mA}$
Operating Range (Note 2) $\quad-5.7 \mathrm{~V}$ to -4.2 V
ESD (Note 2)
$\geq 2000 \mathrm{~V}$
Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

## Recommended Operating

## Conditions

Case Temperature ( $\mathrm{T}_{\mathrm{C}}$ )

| Commercial | $0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| :--- | ---: |
| Industrial | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |
| Military | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Supply Voltage (VE) | -5.7 V to -4.2 V |

## Commercial Version

## DC Electrical Characteristics

$\mathrm{V}_{\mathrm{EE}}=-4.2 \mathrm{~V}$ to $-5.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCA}}=\mathrm{GND}, \mathrm{T}_{\mathrm{C}}=0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | -1025 | -955 | -870 | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\mathrm{Max})} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\text { Min })} \end{aligned}$ | Loading with$50 \Omega \text { to }-2.0 \mathrm{~V}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage | -1830 | -1705 | -1620 |  |  |  |
| $\mathrm{V}_{\mathrm{OHC}}$ | Output HIGH Voltage | -1035 |  |  | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\mathrm{Min})} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\operatorname{Max})} \end{aligned}$ | Loading with$50 \Omega \text { to }-2.0 \mathrm{~V}$ |
| $\mathrm{V}_{\text {OLC }}$ | Output LOW Voltage |  |  | -1610 |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Single-Ended Input HIGH Voltage | -1165 |  | -870 | mV | Guaranteed HIGH Signal for All Inputs |  |
| $\mathrm{V}_{\text {IL }}$ | Single-Ended Input LOW Voltage | -1830 |  | -1475 | mV | Guaranteed LOW Signal for All Inputs |  |
| IIL | Input LOW Current | 0.50 |  |  | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {IN }}=\mathrm{V}_{\text {IL( }}$ Min) |  |
| $\mathrm{IIH}^{\text {H }}$ | Input High Current CLKIN, CLKIN TCLK CLKSEL |  |  | $\begin{aligned} & 150 \\ & 250 \\ & 250 \end{aligned}$ | $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\mathrm{Max})}$ |  |
| $\mathrm{V}_{\text {DIFF }}$ | Input Voltage Differential | 150 |  |  | mV | Required for Full Output Swing |  |
| $\mathrm{V}_{\mathrm{CM}}$ | Common Mode Voltage | $\mathrm{V}_{\mathrm{CC}}-2 \mathrm{~V}$ |  | $\mathrm{V}_{C C}-0.5 \mathrm{~V}$ | V |  |  |
| $\mathrm{I}_{\text {CBO }}$ | Input Leakage Current | -10 |  |  | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{EE}}$ |  |
| $\mathrm{I}_{\mathrm{EE}}$ | Power Supply Current | -67 |  | -35 | mA |  |  |

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Commercial Version (Continued)
AC Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-4.2 \mathrm{~V}$ to $-4.8 \mathrm{~V}, \mathrm{v}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCA}}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{T}_{\mathrm{C}}=0^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{C}}=+85^{\circ} \mathrm{C}$ |  | Units | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max | Min | Max |  |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum Clock Frequency | 750 |  | 750 |  | 750 |  | MHz |  |
| $\begin{aligned} & \text { tpLH } \\ & \mathrm{t}_{\mathrm{pHL}} \end{aligned}$ | Propagation Delay CLKIN, <br> $\overline{\mathrm{CLKIN}}$ to $\mathrm{CLK}_{(1-4)}, \overline{\mathrm{CLK}}_{(1-4)}$ <br> Differential <br> Single-Ended | $\begin{aligned} & 0.59 \\ & 0.59 \end{aligned}$ | $\begin{aligned} & 0.79 \\ & 0.99 \end{aligned}$ | $\begin{aligned} & 0.62 \\ & 0.62 \end{aligned}$ | $\begin{aligned} & 0.82 \\ & 1.02 \end{aligned}$ | $\begin{aligned} & 0.67 \\ & 0.67 \end{aligned}$ | $\begin{aligned} & 0.87 \\ & 1.07 \end{aligned}$ | ns | Figures 1, 3 |
| $t_{\text {PLH }}$ <br> tpHL | Propagation Delay, TCLK to $\operatorname{CLK}_{(1-4)}, \overline{\operatorname{CLK}}_{(1-4)}$ | 0.50 | 1.20 | 0.50 | 1.20 | 0.50 | 1.20 | ns | Figures 1, 2 |
| tpLH $\mathrm{t}_{\mathrm{PHL}}$ | Propagation Delay, CLKSEL to $\operatorname{CLK}_{(1-4)}, \overline{\operatorname{CLK}}_{(1-4)}$ | 0.80 | 1.60 | 0.80 | 1.60 | 0.80 | 1.60 | ns | Figures 1, 2 |
| $\mathrm{t}_{\mathrm{TLH}}$ $\mathrm{t}_{\mathrm{THL}}$ | Transition Time $20 \%$ to $80 \%, 80 \%$ to $20 \%$ | 0.30 | 0.80 | 0.30 | 0.80 | 0.30 | 0.80 | ns | Figures 1, 4 |
| $\begin{aligned} & \text { tost } \\ & \text { DIFF } \end{aligned}$ | Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path |  | 50 |  | 50 |  | 50 | ps | (Note 1) |

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (tOSHL), or LOW to HIGH (tOSLH), or in opposite directions both HL and LH (tost). Parameters tost and tps guaranteed by design.
Industrial Version
DC Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-4.2 \mathrm{~V}$ to $-5.7, \mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCA}}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{T}_{\mathrm{C}}=-40^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{C}}=0^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ |  | Units | Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | -1085 | -870 | -1025 | -870 | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\mathrm{Max})} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\mathrm{Min})} \\ & \hline \end{aligned}$ | Loading with |
| $\mathrm{V}_{\mathrm{OL}}$ | Output LOW Voltage | -1830 | -1575 | -1830 | -1620 | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\operatorname{Min})} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\operatorname{Max})} \end{aligned}$ | $\begin{aligned} & 50 \Omega \text { to } \\ & -2.0 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{OHC}}$ | Output HIGH Voltage | -1095 |  | -1035 |  | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\mathrm{Max})} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\mathrm{Min})} \end{aligned}$ | Loading with |
| $\mathrm{V}_{\text {OLC }}$ | Output LOW Voltage |  | -1565 |  | -1610 | mV | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\text { Min })} \\ & \text { or } \mathrm{V}_{\mathrm{IL}(\mathrm{Max})} \\ & \hline \end{aligned}$ | $\begin{aligned} & 50 \Omega \text { to } \\ & -2.0 \mathrm{~V} \end{aligned}$ |
| $\mathrm{V}_{\mathrm{IH}}$ | Single-Ended Input HIGH Voltage | -1170 | -870 | -1165 | -870 | mV | Guaranteed HIG for All Inputs | Signal |
| VIL | Single-Ended Input LOW Voltage | -1830 | -1480 | -1830 | -1475 | mV | Guaranteed LO for All Inputs | Signal |
| IIL | Input LOW Current | 0.50 |  | 0.50 |  | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\text {ILI(Min) }}$ |  |



## Military Version-Preliminary (Continued)

DC Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-4.2 \mathrm{~V}$ to $-5.7 \mathrm{~V}, \mathrm{v}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCA}}=\mathrm{GND}$ (Note 3) (Continued)

| Symbol | Parameter | Min | Typ | Max | Units | $\mathrm{T}_{\mathrm{C}}$ | Conditions | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {DIFF }}$ | Input Voltage Differential | 150 |  |  | mV | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | Required for Full Output Swing | 1, 2, 3 |
| $\mathrm{V}_{\mathrm{CM}}$ | Common Mode Voltage | $\mathrm{V}_{C C}-2.0$ |  | $V_{C C}-0.5$ | V | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | 1, 2, 3 |
| $\mathrm{V}_{\mathrm{IH}}$ | Single-Ended Input High Voltage | -1165 |  | -870 | mV | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 |
| $\mathrm{V}_{\text {IL }}$ | Single-Ended Input Low Voltage | -1830 |  | -1475 | mV | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 |
| $\mathrm{I}_{\mathrm{IH}}$ | Input HIGH Current CLKIN, $\overline{\text { CLKIN }}$ |  |  | 120 | $\mu \mathrm{A}$ | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}(\text { Max }}$ | 1, 2, 3 |
|  | TCLK |  |  | 350 | $\mu \mathrm{A}$ |  |  |  |
|  | CLKSEL |  |  | 300 | $\mu \mathrm{A}$ |  |  |  |
| $\mathrm{I}_{\text {CBO }}$ | Input Leakage Current | -10 |  |  | $\mu \mathrm{A}$ | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{EE}}$ | 1, 2, 3 |
| ${ }^{\text {EEE }}$ | Power Supply Current, Normal | -90 |  | $-30$ | mA | $\begin{gathered} -55^{\circ} \mathrm{C} \text { to } \\ +125^{\circ} \mathrm{C} \end{gathered}$ |  | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^{\circ} \mathrm{C}$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
Note 2: Screen tested $100 \%$ on each device at $-55^{\circ} \mathrm{C},+25^{\circ} \mathrm{C}$, and $+125^{\circ} \mathrm{C}$, Subgroups $1,2,3,7$, and 8 .
Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^{\circ} \mathrm{C},+25^{\circ} \mathrm{C}$, and $+125^{\circ} \mathrm{C}$, Subgroups A1, 2, 3, 7 , and 8 .
Note 4: Guaranteed by applying specified input condition and testing $\mathrm{V}_{\mathrm{OH}} / \mathrm{V}_{\mathrm{OL}}$.
AC Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-4.2 \mathrm{~V}$ to $-5.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CCA}}=\mathrm{GND}$

| Symbol | Parameter | $\mathrm{T}_{\mathrm{C}}=-55^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{C}}=+25^{\circ} \mathrm{C}$ |  | $\mathrm{T}_{\mathrm{C}}=+125^{\circ} \mathrm{C}$ |  | Units | Conditions | Notes |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max | Min | Max | Min | Max |  |  |  |
| $\begin{aligned} & \text { tPLH } \\ & t_{\text {PHL }} \\ & \hline \end{aligned}$ | Propagation Delay CLKIN, $\overline{\mathrm{CLKIN}}$ to $\mathrm{CLK}_{(1-4)}, \mathrm{CLK}_{(1-4)}$ | 0.61 | 0.81 | 0.61 | 0.81 | 0.60 | 0.83 | ns | Figures 1 and 2 | 1,2, 3 |
| $\begin{aligned} & \mathrm{t}_{\mathrm{PLH}} \\ & \mathrm{t}_{\mathrm{PHL}} \\ & \hline \end{aligned}$ | Propagation Delay, TCLK $\text { to } \mathrm{CLK}_{(1-4)}, \overline{\operatorname{CLK}}_{(1-4)}$ | 0.50 | 1.20 | 0.50 | 1.20 | 0.50 | 1.20 | ns |  |  |
| ts G-G | Skew Gate to Gate (Note 5) |  | 100 |  | 100 |  | 100 | ps |  | 4 |
| $\begin{aligned} & \mathrm{t}_{\mathrm{T} \mathrm{LH}} \\ & \mathrm{t}_{\mathrm{THL}} \\ & \hline \end{aligned}$ | Transition Time $20 \%$ to $80 \%, 80 \%$ to $20 \%$ | 0.35 | 0.80 | 0.30 | 0.75 | 0.25 | 0.75 | ns |  |  |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^{\circ} \mathrm{C}$, then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.
Note 2: Screen tested $100 \%$ on each device at $+25^{\circ} \mathrm{C}$ temperature only, Subgroup A9.
Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^{\circ} \mathrm{C}$, Subgroup A9, and at $+125^{\circ} \mathrm{C}$ and $-55^{\circ} \mathrm{C}$ temperatures, Subgroups A10 and A11.
Note 4: Not tested at $+25^{\circ} \mathrm{C},+125^{\circ} \mathrm{C}$ and $-55^{\circ} \mathrm{C}$ temperature (design characterization data).
Note 5: Maximum output skew for any one device.


TL/F/10960-3
Note 1: Shown for testing CLKIN to CLK1 in the differential mode.
Note 2: L1, L2, L3 and L4 = equal length $50 \Omega$ impedance lines.
Note 3: All unused inputs and outputs are loaded with $50 \Omega$ in parallel with $\leq 3 \mathrm{pF}$ to GND.
Note 4: Scope should have $50 \Omega$ input terminator internally.
FIGURE 1. AC Test Circuit


FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs


FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs


FIGURE 4. Transition Times
Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps .

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:


## Physical Dimensions inches (millimeters)



16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A
100315 Low-Skew Quad Clock Driver

Physical Dimensions inches (millimeters) (Continued)


## LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

| National Semiconductor Corporation <br> 1111 West Bardin Road Arlington, TX 76017 <br> Tel: 1(800) 272-9959 <br> Fax: 1(800) 737-7018 | National Semiconductor Europe <br> Fax: (+49) 0-180-530 8586 <br> Email: cnjwge@tevm2.nsc.com <br> Deutsch Tel: (+49) 0-180-530 8585 <br> English Tel: (+49) 0-180-532 7832 <br> Français Tel: $(+49)$ 0-180-532 9358 <br> Italiano Tel: $(+49)$ 0-180-534 1680 | National Semiconductor Hong Kong Ltd. <br> 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong <br> Tel: (852) 2737-1600 <br> Fax: (852) 2736-9960 | National Semiconductor Japan Ltd. <br> Tel: 81-043-299-2309 <br> Fax: 81-043-299-2408 |
| :---: | :---: | :---: | :---: |


[^0]:    $\mathrm{L}=$ Low Voltage Level
    H = High Voltage Level
    X = Don't Care

